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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THOMSON, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 06/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/159,748	Barrett	
	Examiner	Art Unit	
	Thomson	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *23 September 1998* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/23/98* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

1. Claims 1-11 have been presented for examination. Claims 1-11 have been examined and rejected.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d). A certified copy has been filed in the instant case. Foreign priority date is 09/29/97.

Preamble of the Claims

3. The preamble of the claims presented for examination have not been given patentable weight. Appropriate weight is given to limitations recited in the body of the claim that are needed for the purpose of antecedence. "A mere statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the language of a preamble is necessary to give meaning to the claim" *Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987)*

Specification

4. The disclosure is objected to because of the following informalities:

a. ":-" is recited in a number of locations, for example at line 3, paragraph 1 of the Summary of the Invention.

b. "hereinafter referred to as a BBD" should recite "hereinafter referred to as a BDD, at line 1, Description of the Preferred Embodiments

c. Underlining within the specification should be removed, for example "with variables" at line 2, paragraph 4.

d. The abstract of the disclosure is objected to because it is to be on its own separate sheet. Though it is on a separate sheet it also appears to have a typographic error containing "Fig. 1". Correction is required. See MPEP § 608.01(b)

e. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title is of a generic nature drawn to a family of systems and not to the Applicant's specific claimed invention.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, as recited throughout claims 1-11, the operations of "adapted to arrange the variables", "arranging the variables", "labeling the nodes", and "produce

a list for said labels" must be shown or the feature(s) canceled from the claim(s). It is noted that Figure 6, only shows an arrangement of sets of variables with relationships and related elements of variables from sets. None of the figures explicitly show the operation of generating this arrangement or labeling the nodes or producing a list. Further, the operations of "substituting functions which determine the values of internal signals into the set of functions representing said system", "threshold derived from an original number nodes", "sifting in reverse order", "selected order to a deepest best location followed by sifting in reverse order to a shallowest best location", "detecting an increase in the number of nodes of said binary decision diagram" and "in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. As recited within Applicant's specification, page 5, lines 1 et seq. starting from complete paragraph 4 and at page 9, lines 1-4 in complete paragraph 3, Figures 1,3 and 4 represent the BDD representations of known logic and Figure 2 is a logical diagram of a multiplexer. Applicant explicitly has stated that Figures 5, 6 and 7 are representative of the invention and therefore no modification to them is required. See MPEP § 608.02(g). A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections and Interpretations

7. The following objections to claims are based on 37 C.F.R. § 1.75 (a) and (d) as recited below or appear to be minor grammatical errors:

> (a) The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.
> (d) (1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. (See § 1.58(a)).

8. Claims 1,3, 6-7 objected to because of the following informalities: ":-" after each preamble. This should be replaced with ":". Claim 8 recites "diagram, and , in response" which has been interpreted as "diagram; and in response". Appropriate correction is required.

9. Claims 1-11, recite language that is not clear, descriptive or is ambiguous in nature so as to require the Examiner to decide on the intended meaning when reading and rejecting the claims. Appropriate correction is required.

a. Taking claim 2, for example recites "such that", which has been interpreted to mean that the steps preceding this language yield or provide for the proceeding limitations in some manner.

b. Taking claims 6, for example recites "such detection" has been interpreted to mean "said detection" or "the detection".

c. Taking claim 2, for example recites "a processor adapted to arrange" where the phrase "adapted" has been interpreted "programmed" or alternately "hardwired".

Claim Interpretation

10. Claims having limitations directed to the first storage circuitry, second storage circuitry and processor have been interpreted in view of Applicant's specification page 9, lines 27 et seq. Looking to the prior teachings a SPARCStation inherently has at least one storage circuitry and a processor where storage circuity is based on differing addressable areas of memory. Interpreting Applicant's claims inview of the foregoing: Applicant reads in variables from memory, the processor "consults a function graph by arranging the variables", then outputs to memory the optimized BDD/OBDD, this includes the same memory with different addressable areas of storage.

Claim Rejections - 35 U.S.C. § 112

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, "adapted to arrange the variables", "arranging the variables", "labeling the nodes", "produce a list

for said labels", "sifting in reverse order", "detecting an increase in the number of nodes of said binary decision diagram", "in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph", "said number is a threshold derived from an original number nodes", "substituting functions which determine the values of internal signals into the set of functions representing said system" and "selected order to a deepest best location followed by sifting in reverse order to a shallowest best location" have not been described or taught in a manner so as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Furthermore, the use of the limitations directed to "sifting in reverse order", "detecting an increase in the number of nodes of said binary decision diagram" and "in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph" are not apparent in the specification, less the claims. Looking to the skilled artisan or that person of ordinary skill level in the art; based on the prior art teachings, the aforementioned limitations in view of the specification could not enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention without undue experimentation.

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 4, 5, 6, and 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Specifically, in the recitation of "selected order to a deepest best location followed by sifting in reverse order to a shallowest best location" the use of "best" renders the claim language indefinite. Claim 4 has this same defect. The term "best" in claims 4 and 5 is a relative term which renders the claim indefinite. The term "best" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Claims 6 and 8 recite "depth-first fashion" where the phrase "fashion" renders the claim indefinite. Dependancies from 8 inherit this defect. Claim 7 recites a "depth-first manner" where the phrase "manner" renders the claim indefinite. Claims 6, 7 and 8 do not distinctly point out claim which method is to be used by using the language of "manner" or "fashion" when one comes to the "depth-first" limitation. This language can be interpreted to mean similar or like methodologies to a depth first algorithm. This does not reasonably recite to which specific depth first algorithm is to be implemented. Claims 3, 6 and 7 recite "using said selected order, controlling sifting each variable" is indefinite and probably missing a step after the ",".

CLAIM REJECTIONS UNDER 35 U.S.C. § 101

15. ***The following is a quotation from 35 U.S.C. § 101 which reads as follows***:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-2 are rejected under 35 U.S.C. § 101 as non-statutory subject matter. The invention(s) as disclosed in claims 1-2 are directed to non-statutory subject matter. While the claims are in the technological arts, they are not limited to practical applications in the technological arts and do not result in a anything tangible.

Specifically, the claims are a series of steps to be performed, without a mention of a tangible implementation, but they disclose ideas disclosed abstractly from any particular practical application of graph theory. Specifically, claims 1 and 2 merely recite mathematical algorithms or constructs. This is nothing more than mere manipulation of data relationships with an algorithm. Applicants have not taught a pre or post operation, transformations nor provide any useful outcome, merely an abstraction of data stored in some unknown manner. Though a "list" is produced it represents nothing more than a resulting abstract construct of the algorithm.

To Constitutionally interpret the word "process", the ***Supreme Court*** has held that:

> "*** A process is a mode of treatment of certain materials to produce a given result. It is an act, or a series of acts, performed upon the subject matter to be transformed and reduced to a different state or thing. *** The process requires that *certain things* should be done with *certain substances*, and in a *certain order*; but the tools to be used in doing this may be of secondary consequence." (emphasis added) *Diamond, Commissioner of Patents and Trademarks v. Diehr and Lutton*, 209 USPQ 1, 6 (1981) quoting *Cochrane v. Deener*, 94 U.S. 780, 787-788 (1876).

This Constitutional interpretation of the word "process" is a long-standing one that the Supreme Court requires to be applied in interpreting 35 U.S.C. 101. *Diamond v. Diehr* at 6. Consequently, the use of that interpretation is *Constitutionally required* when we interpret the

Federal Circuit's standard that a "new and useful *process*" is one that produces a "useful, concrete, and tangible result". See, *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 47 USPQ2d 1596, 1600-1601 (Fed. Cir. 1998).

In short, the invention cannot be a "*new and useful* process" if it is not a Constitutional "*process*" in the first place -- regardless of how "useful, concrete, and tangible" one might argue it to be.

Applicant discloses or claims no manipulation of *specific* data representing physical objects or activities (pre-computer activity), nor does it disclose any *specific* independent physical acts being performed by the invention (post-computer activity), less than yielding a "list" of mere abstractions.

The claims merely manipulate abstract ideas in general without limitation to a practical application. Applicant's steps are so disembodied from any process that the Examiner has further attempted to determine if they could be statutory by looking at the claims through the standards defined Alappat-Warmerdam-State Street-AT&T series of cases. Unfortunately, Applicant's claims 1 and 2 have not passed this test.

Both Alappat and State Street involved determinations of whether particular apparatus claims were statutory. AT&T and Warmerdam involved the issues of whether particular method claims were statutory. The analyses in AT&T and Warmerdam are relevant and applicable to the present case because the Federal Circuit has made clear that:

> "Whether stated implicitly or explicitly, **we consider the scope of section 101 to be the same regardless of the form -- machine or process -- in which a particular claim is drafted. ***** (...whether the invention is a process or a machine is irrelevant. The language of the Patent Act itself, as well as **Supreme Court Rulings**, clarifies that

> Alappat's invention fits comfortably within 35 U.S.C. Section 101 whether viewed as a process or a machine.")" AT&T Corp. v. Excel Communications, Inc., 50 USPQ2d 1447, 1451(Fed. Cir. 1999) (emphasis added).

Clearly, the analyses in Warmerdam and AT&T are just as applicable to this case as the analyses in Alappat and State Street. Additionally, The Federal Circuit is clearly looking to and seeking consistency with the Patent Act and *Supreme Court stare decisis*.

Examiner readily finds the uses found by the Federal Circuit in Alappat (the "rasterizer" apparatus) and State Street (the transformation of "discrete dollar values"). Regarding the present case, Examiner seeks a similar **use** to test for concreteness and tangibility.

Following the analytical structure found in both cases, Examiner looks beyond the "apparatus" recital in the claims to find the core use of the mathematics involved. Examiner finds no specific recitations of use in claims 1 and 2. Abstract data is only manipulated with the algorithm, not transformed, in the instant claimed invention as recited in claims 1 and 2. Thought the specification alludes to a probable use, it has not been expressed in the claims with respect to implementing these abstractions with or in such a use to provide a useful outcome. Examiner does understand how such a BDD is used for many differing environments therefore the intended utility or useful test can be overcome.

Since the Warmerdam standards are just as applicable to apparatus or system claims as they are to process claims, Examiner looks to the rule that the act of "taking several abstract ideas and manipulating them together adds nothing to the basic equation." *AT&T v. Excel* at 1453 quoting *In re Warmerdam*, 33 F.3d 1354, 1360 (Fed. Cir. 1994).

The Examiner must treat each claim as a whole. The mere fact that a hardware element is recited in a claim does not necessarily limit the claim to a specific machine or manufacture. cf. In re Iwahashi, 888 F.2d 1370, 1374-75, 12 USPQ2d 1908, 1911-12 (Fed. Cir. 1989), cited with approval in Alappat, 33 F.3d at 1544 n.24, 31 USPQ2d at 1558 n.24.

Therefore, in reviewing the instant claims the following were specifically applied. An invention which is eligible for patenting under 35 U.S.C. § 101 is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The fundamental test for patent eligibility is thus to determine whether the claimed invention produces a "useful, concrete and tangible result." The test for practical application as applied by the examiner involves the determination of the following factors:

(1) "Useful" - The Supreme Court in *Diamond v. Diehr* requires that the examiner look at the claimed invention as a whole and compare any asserted utility with the claimed invention to determine whether the asserted utility is accomplished. Applying utility case law the examiner will note that:

(a) the utility need not be expressly recited in the claims, rather it may be inferred.

(b) if the utility is not asserted in the written description, then it must be well established.

(2) "Tangible" - Applying *In re Warmerdam*, 33 F.3d 1354, 31 USPQ2d 1754 (Fed. Cir. 1994), the examiner will determine whether there is simply a mathematical

construct claimed, such as a disembodied data structure and method of making it. If so, the claim involves no more than a manipulation of an abstract idea and therefore, is nonstatutory under 35 U.S.C. § 101. In *Warmerdam* the abstract idea of a data structure became capable of producing a useful result when it was fixed in a tangible medium which enabled its functionality to be realized.

(3) "Concrete" - Another consideration is whether the invention produces a "concrete" result. Usually, this question arises when a result cannot be assured. An appropriate rejection under 35 U.S.C. § 101 is accompanied by a lack of enablement rejection, because the invention cannot operate as intended without undue experimentation.

Claims 1 and 2 have been examined in view the these issues and has found that these claims do not meet the standard of being tangible so the claims are non-statutory subject matter. However, with the presumption that Applicant might amend the claims to align them with 101, an art rejection has also been applied against these claims 1 and 2.

Claim Rejections - 35 U.S.C. § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. § 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

17. Claims 1-11 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Rudell (IEEE 1993) and further rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Ashar et al. ('183).

Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC.

Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.

Taking claim 1, for example, Rudell (IEEE 1993) and Ashar et al. ('183) individually disclose:

A method for selecting an order in which to sift variables in a binary decision diagram comprising:

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labeled with the variables of the system such that the set of functions labeling leaves reachable from a node correspond to the set of functions which depend on the variables labeling the node; and (OBDD/BDD)

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order (OBDD/BDD optimizing)

As to claim 2, Ashar et al. ('183) and Rudell (IEEE 1993) individually disclose an apparatus for selecting an order in which to sift variables in a binary decision diagram comprising a first store storing (area in memory) bits representing the variables of the binary decision diagram; (BDD)

a second store; and (second area in memory)

a processor (SPARCStation) adapted to arrange the said variables of said binary decision diagram in a representation of the nodes of a graph in which the nodes are labeled with the variables such that the set of functions labeling leaves reachable from a node corresponds to the set of functions which depend on the variables labeling the node; and to traverse the graph in a depth-first manner such that said processor outputs to said second store a list of said labels in said selected order (BDD/OBDD optimizing, depth-first, DVO, sifting, Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill

and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 3, Ashar et al. ('183) and Rudell (IEEE 1993) individually disclose a method for restructuring a binary decision diagram representative of a hardware system (multiplexer or logic), comprising: (BDD/OBDD optimization)

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labeled with the variables of the system such that the set of functions labeling leaves reachable from a node corresponds to the set of functions which depend on the variables labeling the node; and (BDD/OBDD optimization)

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable (depth first, sifting on a BDD for generating an optimized OBDD, Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance

Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 4, a method as claimed in claim 3 wherein said variables are sifted one-by-one to a deepest best location is taught within Ashar et al. ('183) and Rudell (IEEE 1993). (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 5, a method as claimed in claim 3 wherein said variables are sifted one-by-one is said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location are taught within Ashar et al. ('183) and Rudell (IEEE 1993) (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., dicloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, funcitonal relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparision, 5.3 Dynamic Variable Ordering, 5.4 Performance Imapact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the hieristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 6, Ashar et al. ('183) and Rudell (IEEE 1993) individually disclose an apparatus for restructuring a binary decision diagram comprising:

storage circuitry for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labeled by variables; (BDD/OBDD, optimization, using memory)

a processor (SPARCStation) for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labeled such that the set of functions labeling leaves reachable from a node corresponds to the set of functions which depend on the variables labeling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams; (BDD/OBDD, optimizations, DVO , table swaps for sifting with depth first heuristic ordering)

wherein said sifted binary decision diagram is written by said processor to said storage circuits. (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., dicloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, funcitonal relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparision, 5.3 Dynamic Variable Ordering, 5.4 Performance Imapact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the hieristic order based on depth-first, in the sifing algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a

SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 7, Asher et al. and Rudell (IEEE 1993) individually disclose a method for proving the properties of a hardware system comprising: (BDD/OBDD, logic, multiplexer)

representing said system as binary decision diagrams having a plurality of nodes labeled by variables; (BDD/OBDD)

substituting functions which determine variables of internal signals; (partitioning based on signals)

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labeled with the variables of the system such that the set of functions labeling leaves reachable from a node corresponds to the set of functions which depend on the variables labeling the node; and (OBDD optimization)

traversing the graph in a depth-first manner to produce a list of said labels in a selected order; (using depth first algorithm, DVO)

using said selected order, controlling sifting each variable. (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable

Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 8, Asher et al. and Rudell (IEEE 1993) individually disclose an apparatus for proving the properties of a hardware system comprising:(BDD/OBDD, logic, multiplexer)

storage circuitry for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labeled by variables; (BDD/OBDD, partitioning based on functions)

a processor (SPARCStation) for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph in which the nodes are labeled with the variables of the system such that the set of functions labeling leaves reachable from a node corresponding to the set of functions which depend on the variables labeling the node, traversing the graph in a depth-

first fashion to produce a list of labels in said selected order, and using said selected order controlling sifting of the variables of said binary decision diagram; and (BDD/OBDD, DVO, depth first, sifting)

further comprising a second store, wherein said sifting binary decision diagram is written by said processor to said second store. (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 9, an apparatus as claimed in claim 8 wherein said number is a threshold derived from an original number of nodes is taught within Ashar et al. ('183) and Rudell (IEEE 1993) (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the

Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 10, an apparatus as claimed in claim 8 wherein said number of nodes is the number of nodes which branches on a predetermined variable is taught within Ashar et al. ('183) and Rudell (IEEE 1993) (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1

Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

As to claim 11, an apparatus claimed in claim 8 wherein said number is an absolute number is taught within Ashar et al. ('183) and Rudell (IEEE 1993) (Ashar et al. ('183): Abstract, Figure 1, Background of the Invention, col. 1, lines 13-23, Summary of the Invention, col. 2, line 37-col. 3, line 41, col. 4, lines 1-40, col. 6, lines 12 et seq., col. 7, lines 63 et seq., discloses the use of sifting (and its variation), breadth first, and depth first ordering, DVO, multiplexer circuitry model and using partitioning based on signal relationships, functional relationships or flow relationships on a SPARC; Rudell (IEEE 1993): Abstract, sections entitled: 1 Introduction, 3 Dynamic Variable Ordering, 4 Variable Reordering Algorithms, 4.1 Efficient Variable Swap, 4.3 Sifting Algorithm, 5.1 Random Orders vs. Heuristic Orders, 5.2 OBDD Minimization Comparison, 5.3 Dynamic Variable Ordering, 5.4 Performance Impact, and Summary, Conclusion, pages 42-47, note the use of DVO/Heuristic in Table 3, sifting algorithm implemented with dynamic variable ordering and includes the heuristic order based on depth-first, in the sifting algorithm the variables are sifted up to the top, in an up-hill and pair wise swaps based on position, run on a SPARCStation the BDD is optimized on a processor

that reads in the initial BDD from memory and outputs the optimized - ordered BDD (OBDD) to memory.)

Conclusion

18. The prior art made of record, see PTO 892, and not relied upon is considered pertinent to Applicant's disclosure, careful consideration should be given prior to Applicant's response to this Office Action.

19. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this action. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C. 133, M.P.E.P. 710.02, 710.02(b)).

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Thomson whose telephone number is (703) 305-0022. The examiner can be usually reached between 9:30 a.m. - 4:00 p.m. Monday thru Friday. Voice mail is checked throughout the day. Please leave a detailed message including the serial number.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Kevin Teska, can be reached on 704-305-9704. The fax phone number for this Group is 703-308-1396.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 703-305-3900.

William D. Thomson

Patent Examiner

A.U. 2123
May 30, 2002